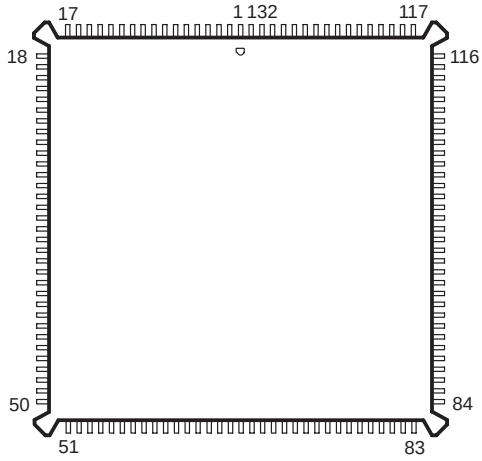
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **Military Operating Temperature Range: −55°C to 125°C**
- **Industrial Operating Temperature Range: −40°C to 85°C**
- **Fast Instruction Cycle Time (30 ns and 40 ns) and 25 ns for Industrial Temp Range**
- **Source-Code Compatible With All TMS320C1x and TMS320C2x Devices**
- **RAM-Based Operation**
  - **9K × 16-Bit Single-Cycle On-Chip Program/Data RAM**
  - **1056 × 16-Bit Dual-Access On-Chip Data RAM**
- **2K × 16-Bit On-Chip Boot ROM**
- **224K × 16-Bit Maximum Addressable External Memory Space (64K Program, 64K Data, 64K I/O, and 32K Global)**
- **32-Bit Arithmetic Logic Unit (ALU)**
  - **32-bit Accumulator (ACC)**
  - **32-Bit Accumulator Buffer (ACCB)**
- **16-Bit Parallel Logic Unit (PLU)**
- **16 × 16-Bit Multiplier, 32-Bit Product**
- **11 Context-Switch Registers**
- **Two Buffers for Circular Addressing**

PQ PACKAGE
(TOP VIEW)



- **Full-Duplex Synchronous Serial Port**
- **Time-Division Multiplexed Serial Port (TDM)**
- **Timer With Control and Counter Registers**
- **16 Software-Programmable Wait-State Generators**
- **Divide-by-One Clock Option**
- **IEEE 1149.1‡ Boundary Scan Logic**
- **Operations Are Fully Static**
- **Enhanced Performance Implanted CMOS (EPIC™) Technology Fabricated by Texas Instruments**
- **Packaging**
  - **132-Lead Plastic Quad Flat Package (PQ Suffix)**

description

The SM320C50-EP digital signal processor (DSP) is a high-performance, 16-bit, fixed-point processor manufactured in 0.72-µm double-level metal CMOS technology. The C50 is the first DSP from TI designed as a fully static device. Full-static CMOS design contributes to low power consumption while maintaining high performance, making it ideal for applications such as battery-operated communications systems, satellite systems, and advanced control algorithms.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

‡ EEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture

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description (continued)

A number of enhancements to the basic C2x architecture give the C50 a minimum 2× performance over the previous generation. A four-deep instruction pipeline, that incorporates delayed branching, delayed call to subroutine, and delayed return from subroutine, allows the C50 to perform instructions in fewer cycles. The addition of a parallel logic unit (PLU) gives the C50 a method for manipulating bits in data memory without using the accumulator and ALU. The C50 has additional shifting and scaling capability for proper alignment of multiplicands or storage of values to data memory.

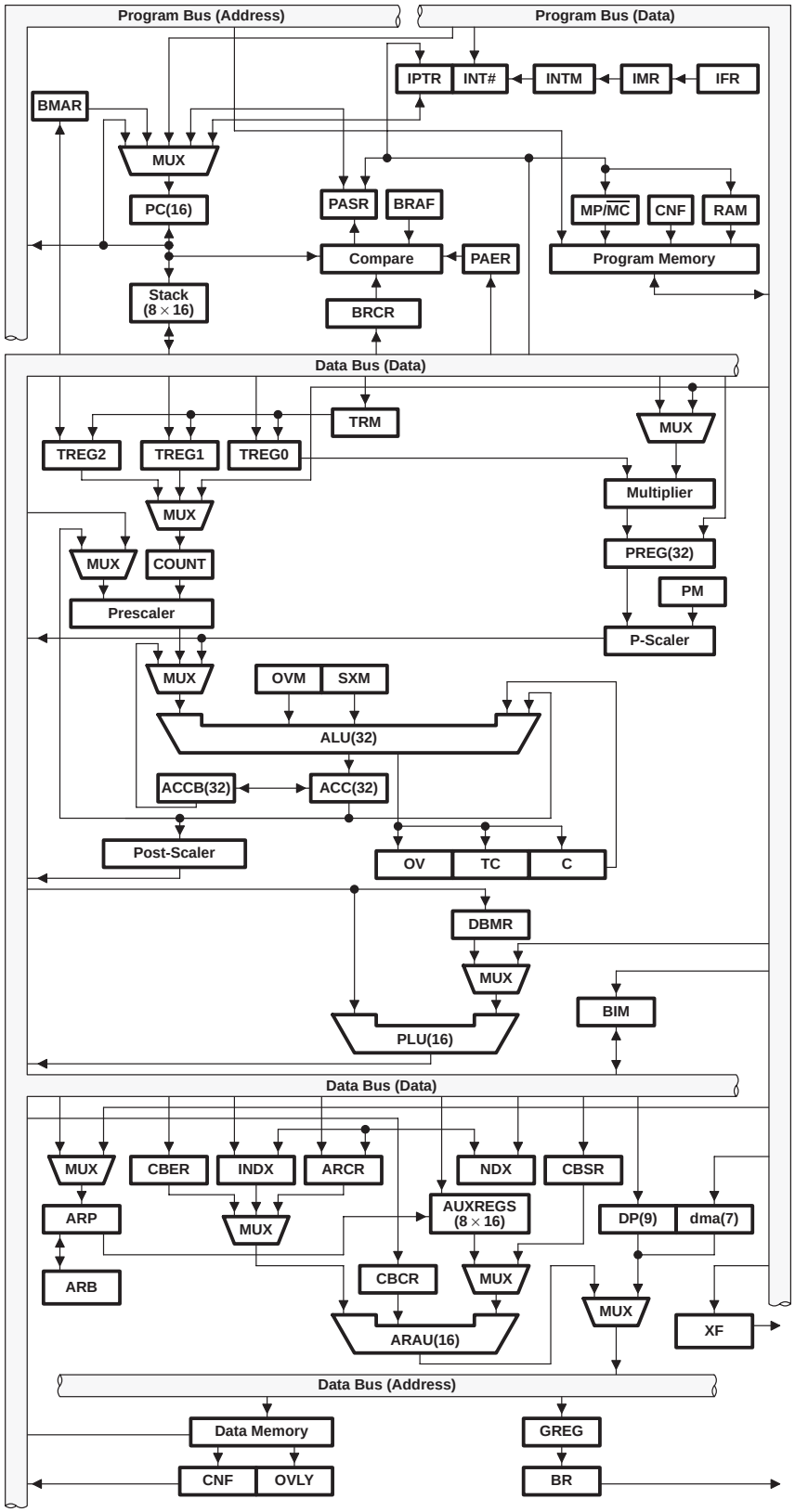
The C50 achieves its low-power consumption through the IDLE2 instruction. IDLE2 removes the functional clock from the internal hardware of the C50, which puts it into a total-sleep mode that uses only 7 μA. A low-logic level on an external interrupt with a duration of at least five clock cycles ends the IDLE2 mode.

The SM320C50-EP is available with a clock speed of 66 MHz providing a 30-ns cycle time and a clock speed of 80 MHz providing a 25-ns cycle time. The available options are listed in Table 1.

Table 1. Available Options

PART NUMBER	SPEED	SUPPLY VOLTAGE TOLERANCE	PACKAGE
SM320C50PQM66EP	30 ns cycle time	±5%	Plastic Quad flat package
SM320C50PQI80EP	25 ns cycle time	±5%	Plastic Quad flat package

functional block diagram



terminal assignments

Table 2. Terminal Assignments (PQ PKG)

TERMINAL NAME	NO.	TERMINAL NAME	NO.	TERMINAL NAME	NO.	TERMINAL NAME	NO.
NC†	18	A2	57	X2/CLKIN	96	TCLKX	123
NC†	19	A3	58	X1	97	CLKX	124
V_{SS3}	20	A4	59	V_{DD11}	98	TFSR/TADD	125
V_{SS4}	21	A5	60	V_{DD12}	99	TCLKR	126
NC†	22	A6	61	TDO	100	$\overline{RS}$	127
D7	23	A7	62	V_{SS13}	101	READY	128
D6	24	A8	63	V_{SS14}	102	$\overline{HOLD}$	129
D5	25	A9	64	CLKMD2	103	$\overline{BIO}$	130
D4	26	V_{DD7}	65	FSX	104	V_{DD15}	131
D3	27	V_{DD8}	66	TFSX/TFRM	105	V_{DD16}	132
D2	28	TDI	67	DX	106	$\overline{IAQ}$	1
D1	29	V_{SS9}	68	TDX	107	$\overline{TRST}$	2
D0(LSB)	30	V_{SS10}	69	$\overline{HOLDA}$	108	V_{SS1}	3
TMS	31	NC†	70	XF	109	V_{SS2}	4
V_{DD3}	32	CLKMD1	71	CLKOUT1	110	MP/$\overline{MC}$	5
V_{DD4}	33	A10	72	NC†	111	D15(MSB)	6
TCK	34	A11	73	$\overline{IACK}$	112	D14	7
V_{SS5}	35	A12	74	V_{DD13}	113	D13	8
V_{SS6}	36	A13	75	V_{DD14}	114	D12	9
NC†	37	A14	76	NC†	115	D11	10
$\overline{INT1}$	38	A15(MSB)	77	NC†	116	D10	11
$\overline{INT2}$	39	NC†	78	NC†	117	D9	12
$\overline{INT3}$	40	NC†	79	EMU0	118	D8	13
$\overline{INT4}$	41	V_{DD9}	80	EMU1/$\overline{OFF}$	119	V_{DD1}	14
$\overline{NMI}$	42	V_{DD10}	81	V_{SS15}	120	V_{DD2}	15
DR	43	$\overline{RD}$	82	V_{SS16}	121	NC†	16
TDR	44	$\overline{WE}$	83	TOUT	122	NC†	17
FSR	45	NC†	84				
CLKR	46	NC†	85				
V_{DD5}	47	V_{SS11}	86				
V_{DD6}	48	V_{SS12}	87				
NC†	49	NC†	88				
NC†	50	$\overline{DS}$	89				
NC†	51	$\overline{IS}$	90				
NC†	52	$\overline{PS}$	91				
V_{SS7}	53	R/$\overline{W}$	92				
V_{SS8}	54	$\overline{STRB}$	93				
A0	55	$\overline{BR}$	94				
A1	56	CLKIN2	95				

† NC = No internal connection

Terminal Functions

TERMINAL NAME	TERMINAL TYPE†	DESCRIPTION
ADDRESS AND DATA BUSES		
A15 (MSB) A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 (LSB)	I/O/Z	Parallel address bus. Multiplexed to address external data, program memory, or I/O. A0−A15 are in the high-impedance state in hold mode and when $\overline{OFF}$ is active (low). These signals are used as inputs for external DMA access of the on-chip single-access RAM. They become inputs while $\overline{HOLDA}$ is active (low) if $\overline{BR}$ is driven low externally.
D15 (MSB) D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 (LSB)	I/O/Z	Parallel data bus. Multiplexed to transfer data between the core CPU and external data, program memory, or I/O devices. D0−D15 are in the high-impedance state when not outputting data, when $\overline{RS}$ or $\overline{HOLD}$ is asserted, or when $\overline{OFF}$ is active (low). These signals also are used in external DMA access of the on-chip single-access RAM.
MEMORY CONTROL SIGNALS		
$\overline{DS}$ $\overline{PS}$ $\overline{IS}$	O/Z	Data, program, and I/O space select signals. Always high unless asserted for communicating to a particular external space. $\overline{DS}$, $\overline{PS}$, and $\overline{IS}$ are in the high-impedance state in hold mode or when $\overline{OFF}$ is active (low).
READY	I	Data ready input. Indicates that an external device is prepared for the bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again. READY also indicates a bus grant to an external device after a $\overline{BR}$ (bus request) signal.
R/$\overline{W}$	I/O/Z	Read/write. R/$\overline{W}$ indicates transfer direction during communication to an external device and is normally in read mode (high) unless asserted for performing a write operation. R/$\overline{W}$ is in the high-impedance state in hold mode or when $\overline{OFF}$ is active (low). Used in external DMA access of the 9K RAM cell, this signal indicates the direction of the data bus for DMA reads (high) and writes (low) when $\overline{HOLDA}$ and $\overline{IAQ}$ are active (low).
$\overline{STRB}$	I/O/Z	Strobe. Always high unless asserted to indicate an external bus cycle, $\overline{STRB}$ is in the high-impedance state in the hold mode or when $\overline{OFF}$ is active (low). Used in external DMA access of the on-chip single-access RAM and while $\overline{HOLDA}$ and $\overline{IAQ}$ are active (low), $\overline{STRB}$ is used to select the memory access.
$\overline{RD}$	O/Z	Read select. $\overline{RD}$ indicates an active external read cycle and can connect directly to the output enable ($\overline{OE}$) of external devices. This signal is active on all external program, data, and I/O reads. $\overline{RD}$ is in the high-impedance state in hold mode or when $\overline{OFF}$ is active (low).

† I = Input, O = Output, Z = High-Impedance

NOTE: All input pins that are unused should be connected to V_{DD} or an external pullup resistor. The $\overline{BR}$ pin has an internal pullup for performing DMA to the on-chip RAM. For emulation, $\overline{TRST}$ has an internal pulldown, and TMS, TCK, and TDI have internal pullups. EMU0 and EMU1 require external pullups to support emulation.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL TYPE†	DESCRIPTION
MEMORY CONTROL SIGNALS (CONTINUED)		
$\overline{WE}$	O/Z	Write enable. The falling edge indicates that the device is driving the external data bus (D15−D0). Data can be latched by an external device on the rising edge of $\overline{WE}$. This signal is active on all external program, data, and I/O writes. $\overline{WE}$ is in the high-impedance state in hold mode or when $\overline{OFF}$ is active (low).
MULTIPROCESSING SIGNALS		
$\overline{HOLD}$	I	Hold. $\overline{HOLD}$ is asserted to request control of the address, data, and control lines. When acknowledged by the C50, these lines go to the high-impedance state.
$\overline{HOLDA}$	O/Z	Hold acknowledge. $\overline{HOLDA}$ indicates to the external circuitry that the processor is in a hold state and that the address, data, and memory control lines are in the high-impedance state so that they are available to the external circuitry for access to local memory. This signal also goes to the high-impedance state when $\overline{OFF}$ is active (low).
$\overline{BR}$	I/O/Z	Bus request. $\overline{BR}$ is asserted during access of external global data memory space. READY is asserted when the global data memory is available for the bus transaction. $\overline{BR}$ can be used to extend the data memory address space by up to 32K words. $\overline{BR}$ goes to the high-impedance state when $\overline{OFF}$ is active low. $\overline{BR}$ is used in external DMA access of the on-chip single-access RAM. While $\overline{HOLDA}$ is active (low), $\overline{BR}$ is externally driven (low) to request access to the on-chip single-access RAM.
$\overline{IAQ}$	O/Z	Instruction acquisition. Asserted (active) when there is an instruction address on the address bus; goes into the high-impedance state when $\overline{OFF}$ is active (low). $\overline{IAQ}$ is also used in external DMA access of the on-chip single-access RAM. While $\overline{HOLDA}$ is active (low), $\overline{IAQ}$ acknowledges the $\overline{BR}$ request for access of the on-chip single-access RAM and stops indicating instruction acquisition.
$\overline{BIO}$	I	Branch control. $\overline{BIO}$ samples as the BIO condition and, if it is low, causes the device to execute the conditional instruction. $\overline{BIO}$ must be active during the fetch of the conditional instruction.
XF	O/Z	External flag (latched software-programmable signal). Set high or low by a specific instruction or by loading status register 1 (ST1). Used for signaling other processors in multiprocessor configurations or as a general-purpose output. XF goes to the high-impedance state when $\overline{OFF}$ is active (low) and is set high at reset.
$\overline{IACK}$	O/Z	Interrupt acknowledge. Indicates receipt of an interrupt and that the program counter is fetching the interrupt vector location designated by A15−A0. $\overline{IACK}$ goes to the high-impedance state when $\overline{OFF}$ is active (low).
INITIALIZATION, INTERRUPT, AND RESET OPERATIONS		
$\overline{INT4}$ $\overline{INT3}$ $\overline{INT2}$ $\overline{INT1}$	I	External interrupts. $\overline{INT1}$−$\overline{INT4}$ are prioritized and maskable by the interrupt mask register (IMR) and interrupt mode bit (INTM, bit 9 of status register 0). These signals can be polled and reset by using the interrupt flag register.
$\overline{NMI}$	I	Nonmaskable interrupt. $\overline{NMI}$ is the external interrupt that cannot be masked via INTM or IMR. When $\overline{NMI}$ is activated, the processor traps to the appropriate vector location.
$\overline{RS}$	I	Reset. $\overline{RS}$ causes the device to terminate execution and forces the program counter to zero. When $\overline{RS}$ is brought to a high level, execution begins at location zero of program memory.
MP/$\overline{MC}$	I	Microprocessor/microcomputer select. If active (low) at reset (microcomputer mode), the signal causes the internal program ROM to be mapped into program memory space. In the microprocessor mode, all program memory is mapped externally. This signal is sampled only during reset, and the mode that is set at reset can be overridden via the software control bit MP/$\overline{MC}$ in the PMST register.
OSCILLATOR/TIMER SIGNALS		
CLKOUT1	O/Z	Master clock (or CLKIN2 frequency). CLKOUT1 cycles at the machine-cycle rate of the CPU. The internal machine cycle is bounded by the rising edges of this signal. This signal goes to the high-impedance state when $\overline{OFF}$ is active (low).

† I = Input, O = Output, Z = High-Impedance

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL TYPE†	DESCRIPTION
OSCILLATOR/TIMER SIGNALS (CONTINUED)		
CLKMD1 CLKMD2	I	CLKMD1 = 0, CLKMD2 = 0: External clock with divide-by-two option. Input clock is provided to X2/CLKIN1. Internal oscillator and PLL are disabled. CLKMD1 = 0, CLKMD2 = 1: Reserved for test purposes CLKMD1 = 1, CLKMD2 = 0: External divide-by-one option. Input clock is provided to CLKIN2. Internal oscillator is disabled and internal PLL is enabled. CLKMD1 = 1, CLKMD2 = 1: Internal or external divide-by-two option. Input clock is provided to X2/CLKIN1. Internal oscillator is enabled and internal PLL is disabled.
X2/CLKIN	I	Input to the internal oscillator from the crystal. If the internal oscillator is not being used, a clock can be input to the device on X2/CLKIN. The internal machine cycle is half this clock rate.
X1	O	Output from the internal oscillator for the crystal. If the internal oscillator is not used, X1 must be left unconnected. This signal does not go to the high-impedance state when $\overline{OFF}$ is active (low).
CLKIN2	I	Divide-by-one input clock for driving the internal machine rate.
TOUT	O	Timer output. TOUT signals a pulse when the on-chip timer counts down past zero. The pulse is a CLKOUT1 cycle wide.
SUPPLY PINS		
V_{DD1} V_{DD2} V_{DD3} V_{DD4}	I	Power supply for data bus
V_{DD5} V_{DD6}	I	Power supply for address bus
V_{DD7} V_{DD8}	I	Power supply for inputs and internal logic
V_{DD9} V_{DD10}	I	Power supply for address bus
V_{DD11} V_{DD12}	I	Power supply for memory control signals
V_{DD13} V_{DD14}	I	Power supply for inputs and internal logic
V_{DD15} V_{DD16}	I	Power supply for memory control signals
V_{SS1} V_{SS2}	I	Ground for memory control signals
V_{SS3} V_{SS4} V_{SS5} V_{SS6}	I	Ground for data bus
V_{SS7} V_{SS8} V_{SS9} V_{SS10}	I	Ground for address bus
V_{SS11} V_{SS12}	I	Ground for memory control signals
V_{SS13} V_{SS14} V_{SS15} V_{SS16}	I	Ground for inputs and internal logic

† I = Input, O = Output, Z = High-Impedance

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL TYPE†	DESCRIPTION
SERIAL PORT SIGNALS		
CLKR TCLKR	I	Receive clock. External clock signal for clocking data from DR (data receive) or TDR (TDM data receive) into the RSR (serial port receive shift register). Must be present during serial port transfers. If the serial port is not being used, these signals can be sampled as an input via the IN0 bit of the serial port control (SPC) or TDR serial port control (TSPC) registers.
CLKX TCLKX	I/O/Z	Transmit clock. Clock signal for clocking data from the DR or TDR to the DX (data transmit) or TDX (TDM data transmit pins). CLKX can be an input if the MCM bit in the serial port control register is set to 0. It can also be driven by the device at 1/4 the CLKOUT1 frequency when the MCM bit is set to 1. If the serial port is not being used, this pin can be sampled as an input via the IN1 bit of the SPC or TSPC register. This signal goes into the high-impedance state when $\overline{\text{OFF}}$ is active (low).
DR TDR	I	Serial data receive. Serial data is received in the RSR (serial port receive shift register) via DR or TDR.
DX TDX	O/Z	Serial port transmit. Serial data transmitted from XSR (serial port transmit shift register) via DX or TDX. This signal is in the high-impedance state when not transmitting and when $\overline{\text{OFF}}$ is active (low).
FSR TFSR/TADD	I I/O/Z	Frame synchronization pulse for receive. The falling edge of FSR or TFSR initiates the data receive process, which begins the clocking of the RSR. TFSR becomes an input/output (TADD) pin when the serial port is operating in the TDM mode (TDM bit = 1). In TDM mode, this pin is used to input/output the address of the port. This signal goes into the high-impedance state when $\overline{\text{OFF}}$ is active (low).
FSX TFSX/TFRM	I/O/Z	Frame synchronization pulse for transmit. The falling edge of FSX/TFSX initiates the data transmit process, which begins the clocking of the XSR. Following reset, the default operating condition of FSX/TFSX is an input. This pin may be selected by software to be an output when the TXM bit in the serial control register is set to 1. This signal goes to the high-impedance state when $\overline{\text{OFF}}$ is active (low). When operating in TDM mode (TDM bit = 1), TFSX becomes TFRM, the TDM frame-synchronization pulse.
TEST SIGNALS		
TCK	I	Boundary scan test clock. This is normally a free-running clock with a 50% duty cycle. The changes of TAP (test access port) input signals (TMS and TDI) are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TDI	I	Boundary scan test data input. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	O/Z	Boundary scan test data output. The contents of the selected register (instruction or data) is shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when scanning of data is in progress. This signal also goes to the high-impedance state when $\overline{\text{OFF}}$ is active (low).
TMS	I	Boundary scan test mode select. This serial control input is clocked into the test access port (TAP) controller on the rising edge of TCK.
$\overline{\text{TRST}}$	I	Boundary scan test reset. Asserting this signal gives the JTAG scan system control of the operations of the device. If this signal is not connected or is driven low, the device operates in its functional mode and the boundary scan signals are ignored.
EMU0	I/O/Z	Emulator 0. When $\overline{\text{TRST}}$ is driven low, EMU0 must be high for activation of the $\overline{\text{OFF}}$ condition (see EMU1/$\overline{\text{OFF}}$). When $\overline{\text{TRST}}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output put via boundary scan.
EMU1/$\overline{\text{OFF}}$	I/O/Z	Emulator 1/$\overline{\text{OFF}}$. When $\overline{\text{TRST}}$ is driven high, EMU1/$\overline{\text{OFF}}$ is used as an interrupt to or from the emulator system and is defined as input/output via boundary scan. When $\overline{\text{TRST}}$ is driven low, EMU1/$\overline{\text{OFF}}$ is configured as $\overline{\text{OFF}}$. When the $\overline{\text{OFF}}$ signal is active (low), all output drivers are in the high-impedance state. $\overline{\text{OFF}}$ is used exclusively for testing and emulation purposes (not for multiprocessing applications). For the $\overline{\text{OFF}}$ condition, the following conditions apply: • $\overline{\text{TRST}}$ = Low • EMU0 = High • EMU1/$\overline{\text{OFF}}$ = Low
RESERVED	N/C	Reserved. This pin must be left unconnected.

† I = Input, O = Output, Z = High-Impedance

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . − 0.3 V to 7 V
Input voltage range . . . . . − 0.3 V to 7 V
Output voltage range . . . . . − 0.3 V to 7 V
Operating case temperature range, T_C . . . . . − 55°C to 125°C
Storage temperature range, T_{stg} . . . . . − 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.75	5	5.25	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	CLKIN, CLKIN2	3		V_{DD} + 0.3	V
		CLKX, CLKR, TCLKX, TCLKR	2.5		V_{DD} + 0.3	V
		All others	2.2		V_{DD} + 0.3	V
V_{IL}	Low-level input voltage		−0.3		0.6	V
I_{OH}	High-level output current				−300‡	µA
I_{OL}	Low-level output current				2	mA
T_C	Operating case temperature (see Note 2)	Mil Temp Parts	−55		125	°C
		Industrial Temp Range	−40		85	°C

‡ This I_{OH} can be exceeded when using a 1-kΩ pulldown resistor on the TDM serial port TADD output; however, this output still meets V_{OH} specifications under these conditions.

NOTE 2: T_C MAX at maximum rated operating conditions at any point on case. T_C MIN at initial (time zero) power up.

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS§			MIN	TYP¶	MAX	UNIT
V_{OH}	High-level output voltage#	I_{OH} = MAX			2.4	3		V
V_{OL}	Low-level output voltage¶	I_{OL} = MAX				0.3	0.6	V
I_{OZ}	High-impedance output current (V_{DD} = MAX)	$\overline{BR}$ (with internal pullup)			−500	‖	30	µA
		All others			−30	‖	30	
I_I	Input current (V_I = V_{SS} to V_{DD})	$\overline{TRST}$ (with internal pulldown)			−30	‖	800	µA
		TMS, TCK, TDI (with internal pullups)			−500	‖	30	
		X2/CLKIN			−50	‖	50	
		All other inputs			−30	‖	30	µA
I_{DDC}	Supply current, core CPU	Operating,	T_A = 25°C,	V_{DD} = 5.25 V, f_x = 66 MHz		60	225	mA
		Operating,	T_A = 25°C,	V_{DD} = 5.25 V, f_x = 66 MHz		94		
I_{DDP}	Supply current, pins	Operating,	T_A = 25°C,	V_{DD} = 5.25 V, f_x = 66 MHz		40	225	mA
		Operating,	T_A = 25°C,	V_{DD} = 5.25 V, f_x = 66 MHz		63		
I_{DD}	Supply current, standby	IDLE instruction,	T_C = 125°C,	V_{DD} = 5.25 V, f_x = 66 MHz			30	mA
		IDLE2 instruction,	Clocks shut off,	V_{DD} = 5.25 V, T_C = 125°C			7	µA
C_i	Input capacitance					15	40	pF
C_o	Output capacitance					15	40	pF

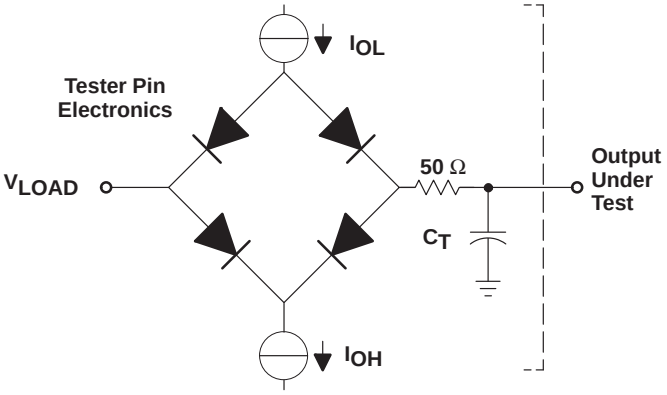
§ For conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

¶ All typical or nominal values are at V_{DD} = 5 V, T_A (ambient air temperature)= 25°C.

All input and output voltage levels are TTL-compatible. Figure 1 shows the test load circuit; Figure 2 and Figure 3 show the voltage reference levels.

‖ These values are not specified pending detailed characterization.

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2.0 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{LOAD} = 1.5 V
C_T = 80 pF typical load circuit capacitance

Figure 1. Test Load Circuit

signal transition levels

Transistor-to-transistor logic (TTL) output levels are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.6 V. Figure 2 shows the TTL-level outputs.

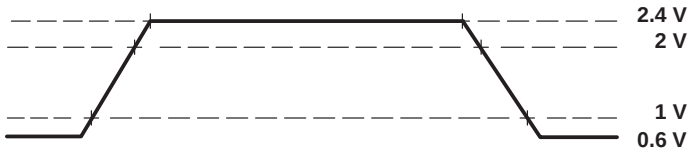


Figure 2. TTL-Level Outputs

TTL-output transition times are specified as follows:

- For a *high-to-low transition*, the level at which the output is said to be no longer high is 2 V, and the level at which the output is said to be low is 1 V.
- For a *low-to-high transition*, the level at which the output is said to be no longer low is 1 V, and the level at which the output is said to be high is 2 V.

Figure 3 shows the TTL-level inputs.



Figure 3. TTL-Level Inputs

TTL-compatible input transition times are specified as follows:

- For a *high-to-low transition* on an input signal, the level at which the input is said to be no longer high is 2 V, and the level at which the input is said to be low is 0.8 V.
- For a low to high transisiton on an input signal, the level at which the input is said to be no longer low is 0.8 V, and the level at which the input is said to be high is 2 V.

CLOCK CHARACTERISTICS AND TIMING

The C50 can use either its internal oscillator or an external frequency source for a clock. The clock mode is determined by the CLKMD1 and CLKMD2 pins. Table 3 outlines the selection of the clock mode by these pins.

Table 3. Clock Mode Selection

CLKMD1	CLKMD2	CLOCK SOURCE
1	0	External divide-by-one clock option
0	1	Reserved for test purposes
1	1	External divide-by-two option or internal divide-by-two clock option with an external crystal
0	0	External divide-by-two option with the internal oscillator disabled

internal divide-by-two clock option with external crystal

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN. The frequency of CLKOUT1 is one-half the crystal oscillating frequency. The crystal should be in either fundamental or overtone operation and parallel resonant, with an effective series resistance of 30 Ω and a power dissipation of 1 mW; it should be specified at a load capacitance of 20 pF. Overtone crystals require an additional tuned LC circuit. Figure 4 shows an external crystal (fundamental frequency) connected to the on-chip oscillator.

recommended operating conditions for internal divide-by-two clock option

		MIN	NOM	MAX	UNIT
f_X	Input clock frequency	0†		66	MHz
C1, C2	Load capacitance		10		pF

† This device uses a fully static design and, therefore, can operate with $t_{C(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz but is tested at a minimum of 3.3 MHz to meet device test time requirements.

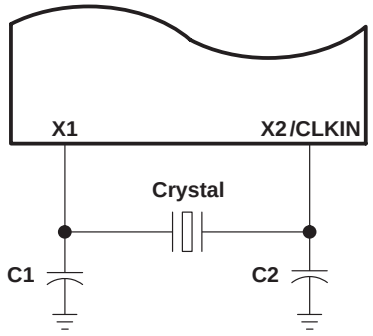


Figure 4. Internal Clock Option

external divide-by-two clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected, CLKMD1 set high, and CLKMD2 set high. The external frequency is divided by two to generate the internal machine cycle. The external frequency injected must conform to specifications listed in the timing requirements table (see Figure 5 for more details).

switching characteristics over recommended operating conditions [H = 0.5 $t_{c(CO)}$]

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(CO)}$	Cycle time, CLKOUT1	30	$2t_{c(CI)}$	†	ns
$t_{d(CIH-COH/L)}$	Delay time, X2/CLKIN high to CLKOUT1 high/low	3	11	20	ns
$t_{f(CO)}$	Fall time, CLKOUT1		5		ns
$t_{r(CO)}$	Rise time, CLKOUT1		5		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low	H − 3	H	H + 2	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high	H − 3	H	H + 2	ns

† This device uses a fully static design and, therefore, can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz, but is tested at a minimum of 6.7 MHz to meet device test time requirements.

timing requirements

		MIN	MAX	UNIT
$t_{c(CI)}$	Cycle time, X2/CLKIN	15	†	ns
$t_{f(CI)}$	Fall time, X2/CLKIN		5*	ns
$t_{r(CI)}$	Rise time, X2/CLKIN		5*	ns
$t_{w(CIL)}$	Pulse duration, X2/CLKIN low	7	†	ns
$t_{w(CIH)}$	Pulse duration, X2/CLKIN high	7	†	ns

† This device uses a fully static design and, therefore, can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz, but is tested at a minimum of 6.7 MHz to meet device test time requirements.

* This parameter is not production tested.

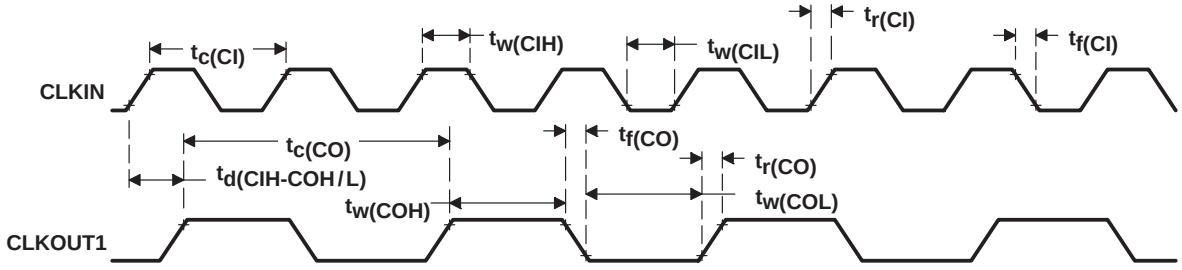


Figure 5. External Divide-by-Two Clock Timing

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external divide-by-one clock option

An external frequency source can be used by injecting the frequency directly into CLKIN2 with X1 left unconnected and X2 connected to V_{DD}. This external frequency is divided by one to generate the internal machine cycle. The divide-by-one option is used when CLKMD1 is strapped high and CLKMD2 is strapped low. The external frequency injected must conform to specifications listed in the timing requirements table (see Figure 6 for more details).

switching characteristics over recommended operating conditions [H = 0.5 $t_{c(CO)}$]

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(CO)}$	Cycle time, CLKOUT1	30	$t_{c(CI)}$	75*	ns
$t_{d(C2H-COH)}$	Delay time, CLKIN2 high to CLKOUT1 high	2	9	16	ns
$t_{f(CO)}$	Fall time, CLKOUT1		5		ns
$t_{r(CO)}$	Rise time, CLKOUT1		5		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low	H − 3*	H	H + 2*	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high	H − 3*	H	H + 2*	ns
$t_{d(TP)}$	Delay time, transitory phase−PLL synchronized after CLKIN2 supplied			1000$t_{c(C2)}$*	ns

* This parameter is not production tested.

timing requirements over recommended ranges of supply voltage and operating case temperature

		MIN	MAX	UNIT
$t_{c(C2)}$	Cycle time, CLKIN2	30	75†	ns
$t_{f(C2)}$	Fall time, CLKIN2		5*	ns
$t_{r(C2)}$	Rise time, CLKIN2		5*	ns
$t_{w(C2L)}$	Pulse duration, CLKIN2 low	9	$t_{c(C2)}$−9	ns
$t_{w(C2H)}$	Pulse duration, CLKIN2 high	9	$t_{c(C2)}$−9	ns

* This parameter is not production tested.

† Clocks can be stopped only while the device executes IDLE2 when using the external divide-by-one clock option. Note that tp (the transitory phase) occurs when restarting clock from IDLE2 in this mode.

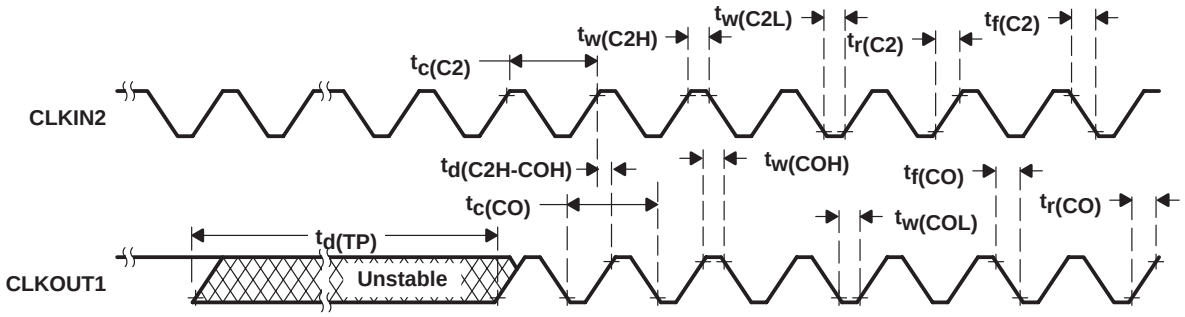


Figure 6. External Divide-by-One Clock Timing

MEMORY AND PARALLEL I/O INTERFACE READ

Memory and parallel I/O interface read timings are illustrated in Figure 7.

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$]

PARAMETER		MIN	MAX	UNIT
$t_{su(AV-RDL)}$	Setup time, address valid before $\overline{RD}$ low	H−10†‡		ns
$t_{h(RDH-AV)}$	Hold time, address valid after $\overline{RD}$ high	0†‡		ns
$t_{w(RDL)}$	Pulse duration, $\overline{RD}$ low	H−2§*		ns
$t_{w(RDH)}$	Pulse duration, $\overline{RD}$ high	H−2§*		ns
$t_{d(RDH-WEL)}$	Delay time, $\overline{RD}$ high to $\overline{WE}$ low	2H−5		ns

† A15−A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in timings referenced as address.
‡ See Figure 8 for address-bus timing variation with load capacitance.
§ $\overline{STRB}$ and $\overline{RD}$ timing is − 3/+5 ns from CLKOUT1 timing on read cycles, following the first cycle after reset, which is always a seven wait-state cycle.
* This parameter is not production tested.

timing requirements [H = 0.5 $t_{c(CO)}$]

		MIN	MAX	UNIT
$t_{a(RDAV)}$	Access time, read data valid from address valid		2H−15‡	ns
$t_{a(RDL-RD)}$	Access time, read data valid after $\overline{RD}$ low		H−10	ns
$t_{su(RD-RDH)}$	Setup time, read data valid before $\overline{RD}$ high	10		ns
$t_{h(RDH-RD)}$	Hold time, read data valid after $\overline{RD}$ high	0		ns

‡ See Figure 8 for address-bus timing variation with load capacitance.

MEMORY AND PARALLEL I/O INTERFACE WRITE

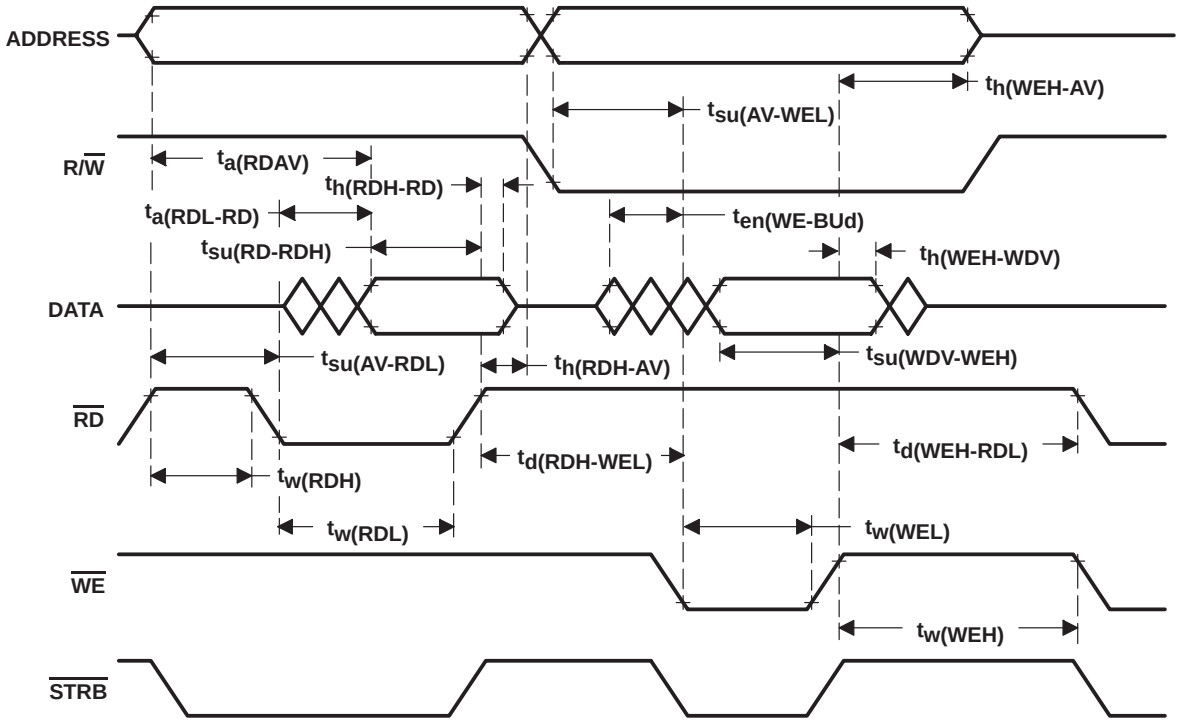
Memory and parallel I/O interface read timings are illustrated in Figure 7.

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$]

PARAMETER		MIN	MAX	UNIT
$t_{su(AV-WEL)}$	Setup time, address valid before $\overline{WE}$ low	H − 5†‡		ns
$t_{h(WEH-AV)}$	Hold time, address valid after $\overline{WE}$ high	H − 10†‡		ns
$t_{w(WEL)}$	Pulse duration, $\overline{WE}$ low	2H − 4¶*	2H + 2¶*	ns
$t_{w(WEH)}$	Pulse duration, $\overline{WE}$ high	2H − 2¶		ns
$t_{d(WEH-RDL)}$	Delay time, $\overline{WE}$ high to $\overline{RD}$ low	3H − 10		ns
$t_{su(WDV-WEH)}$	Setup time, write data valid before $\overline{WE}$ high	2H − 20¶*	2H¶#*	ns
$t_{h(WEH-WDV)}$	Hold time, write data valid after $\overline{WE}$ high	H − 5¶*	H+10¶*	ns
$t_{en(WE-BUd)}$	Enable time, $\overline{WE}$ to data bus driven	−5*		ns

† A15−A0,$\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in timings referenced as address.
‡ See Figure 8 for address-bus timing variation with load capacitance.
¶ $\overline{STRB}$ and $\overline{WE}$ edges are 0−4 ns from CLKOUT1 edges on writes. Rising and falling edges of these signals track each other; tolerance of resulting pulse durations is ± 2 ns, not ± 4 ns.
# This value holds true for zero or one wait state only.
* This parameter is not production tested.

MEMORY AND PARALLEL I/O INTERFACE WRITE



NOTE A: All timings are for 0 wait states. However, external writes always require two cycles to prevent external bus conflicts. The above diagram illustrates a one-cycle read and a two-cycle write and is not drawn to scale. All external writes immediately preceded by an external read or immediately followed by an external read require three machine cycles.

Figure 7. Memory and Parallel I/O Interface Read and Write Timing

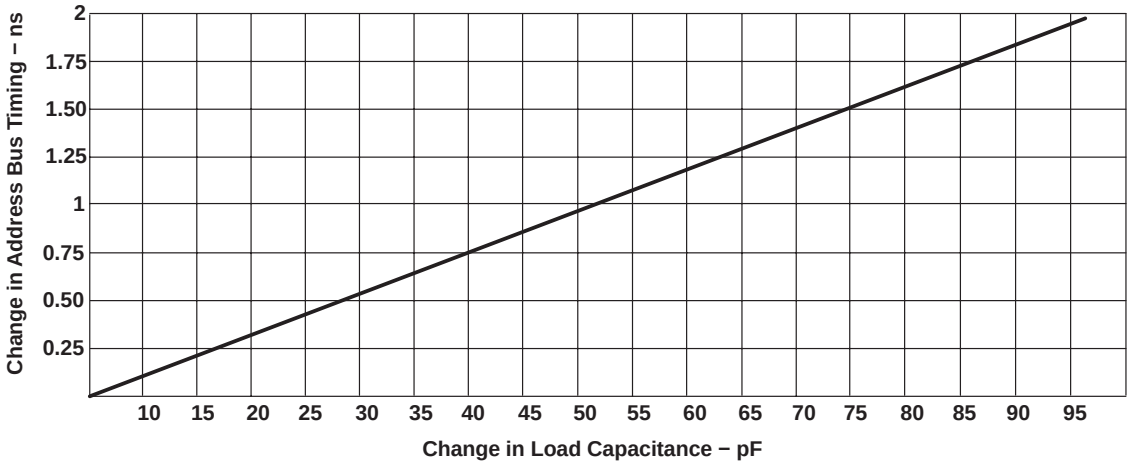


Figure 8. Address Bus Timing Variation With Load Capacitance

READY TIMING FOR EXTERNALLY GENERATED WAIT STATES

timing requirements [H = 0.5$t_{c(CO)}$] (see Figure 9 and Figure 10)

		MIN	MAX	UNIT
$t_{su(RY-COH)}$	Setup time, READY before CLKOUT1 rises	10		ns
$t_{h(CO-RYH)}$	Hold time, READY after CLKOUT1 rises	0		ns
$t_{su(RY-RDL)}$	Setup time, READY before $\overline{RD}$ falls	10		ns
$t_{h(RDL-RY)}$	Hold time, READY after $\overline{RD}$ falls	0		ns
$t_{v(WEL-RY)}$	Valid time, READY after $\overline{WE}$ falls	H − 15		ns
$t_{h(WEL-RY)}$	Hold time, READY after $\overline{WE}$ falls	H + 5		ns

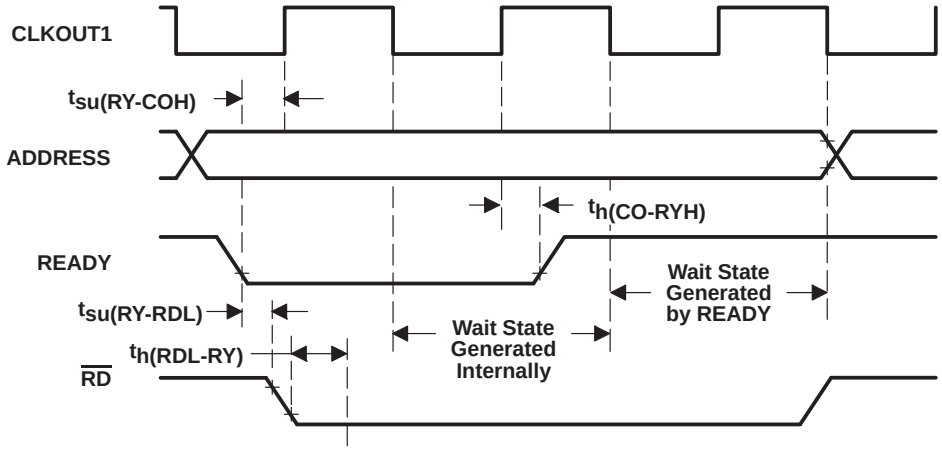


Figure 9. Ready Timing for Externally Generated Wait States During an External Read Cycle

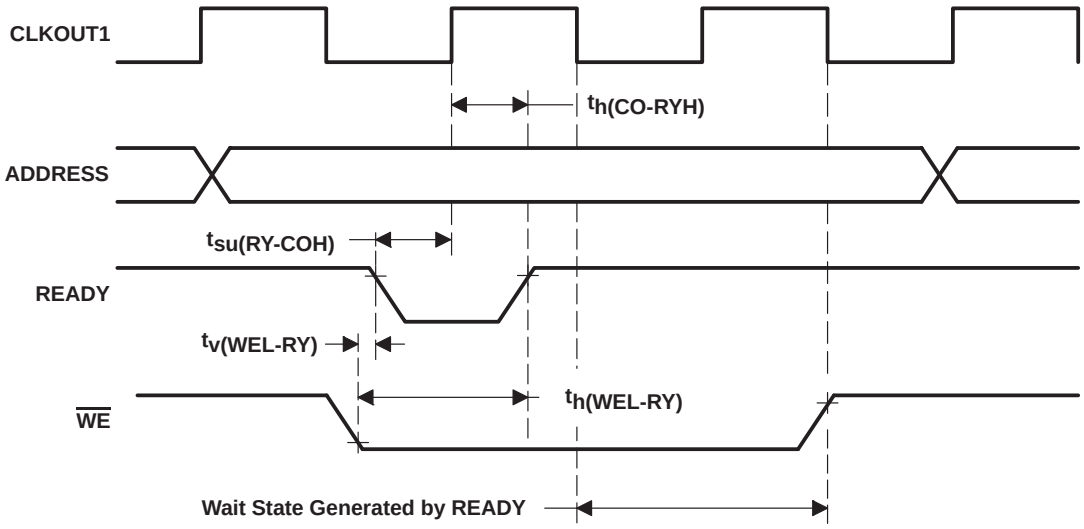


Figure 10. Ready Timing for Externally Generated Wait States During an External Write Cycle

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RESET, INTERRUPT, AND $\overline{\text{BIO}}$

timing requirements [H = 0.5$t_{c(CO)}$] (see Figure 11)

		MIN	MAX	UNIT
$t_{su(IN-COL)}$	Setup time, $\overline{\text{INT1}}$−$\overline{\text{INT4}}$, $\overline{\text{NMI}}$, before CLKOUT1 low †	15		ns
$t_{h(COL-IN)}$	Hold time, $\overline{\text{INT1}}$−$\overline{\text{INT4}}$, $\overline{\text{NMI}}$, after CLKOUT1 low †	0		ns
$t_{w(INL)SYN}$	Pulse duration, $\overline{\text{INT1}}$−$\overline{\text{INT4}}$, $\overline{\text{NMI}}$ low, synchronous	4H+15‡		ns
$t_{w(INH)SYN}$	Pulse duration, $\overline{\text{INT1}}$−$\overline{\text{INT4}}$, $\overline{\text{NMI}}$ high, synchronous	2H+15‡*		ns
$t_{w(INL)ASY}$	Pulse duration, $\overline{\text{INT1}}$−$\overline{\text{INT4}}$, $\overline{\text{NMI}}$ low, asynchronous	6H+15‡*		ns
$t_{w(INH)ASY}$	Pulse duration, $\overline{\text{INT1}}$−$\overline{\text{INT4}}$, $\overline{\text{NMI}}$ high, asynchronous	4H+15‡*		ns
$t_{su(RS-X2L)}$	Setup time, $\overline{\text{RS}}$ before X2/CLKIN low	10		ns
$t_{w(RSL)}$	Pulse duration, $\overline{\text{RS}}$ low	12H		ns
$t_{d(RSH)}$	Delay time, $\overline{\text{RS}}$ high to reset vector fetch	34H		ns
$t_{w(BIL)SYN}$	Pulse duration, $\overline{\text{BIO}}$ low, synchronous	15		ns
$t_{w(BIL)ASY}$	Pulse duration, $\overline{\text{BIO}}$ low, asynchronous	H+15*		ns
$t_{su(BI-COL)}$	Setup time, $\overline{\text{BIO}}$ before CLKOUT1 low	15		ns
$t_{h(COL-BI)}$	Hold time, $\overline{\text{BIO}}$ after CLKOUT1 low	0		ns

† These parameters must be met to use the synchronous timings. Both reset and the interrupts can operate asynchronously. The pulse durations require an extra half-cycle to assure internal synchronization.
‡ If in IDLE2, add 4H to these timings.
*This parameter is not production tested.

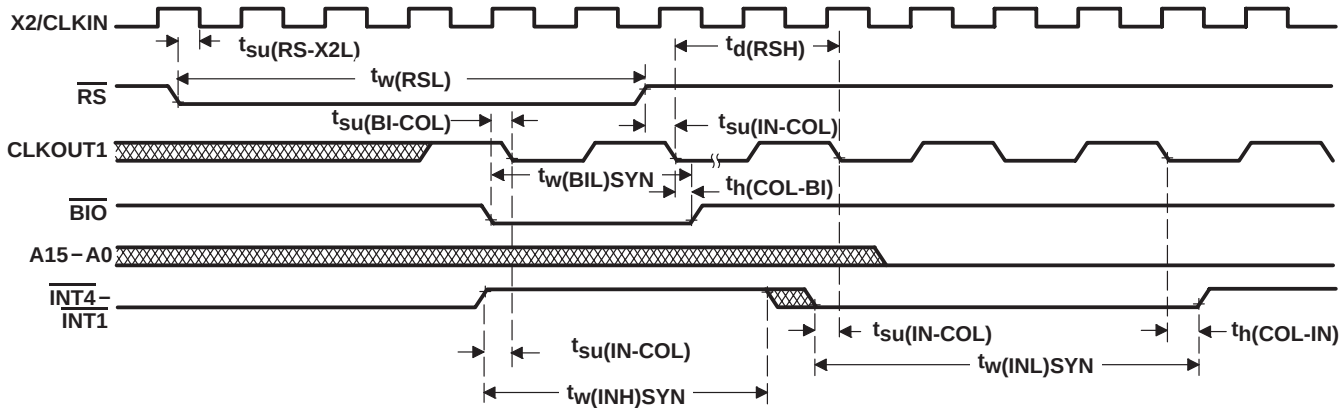


Figure 11. Reset, Interrupt, and $\overline{\text{BIO}}$ Timings

INSTRUCTION ACQUISITION ($\overline{IAQ}$), INTERRUPT ACKNOWLEDGE ($\overline{IACK}$), EXTERNAL FLAG (XF), AND TOUT

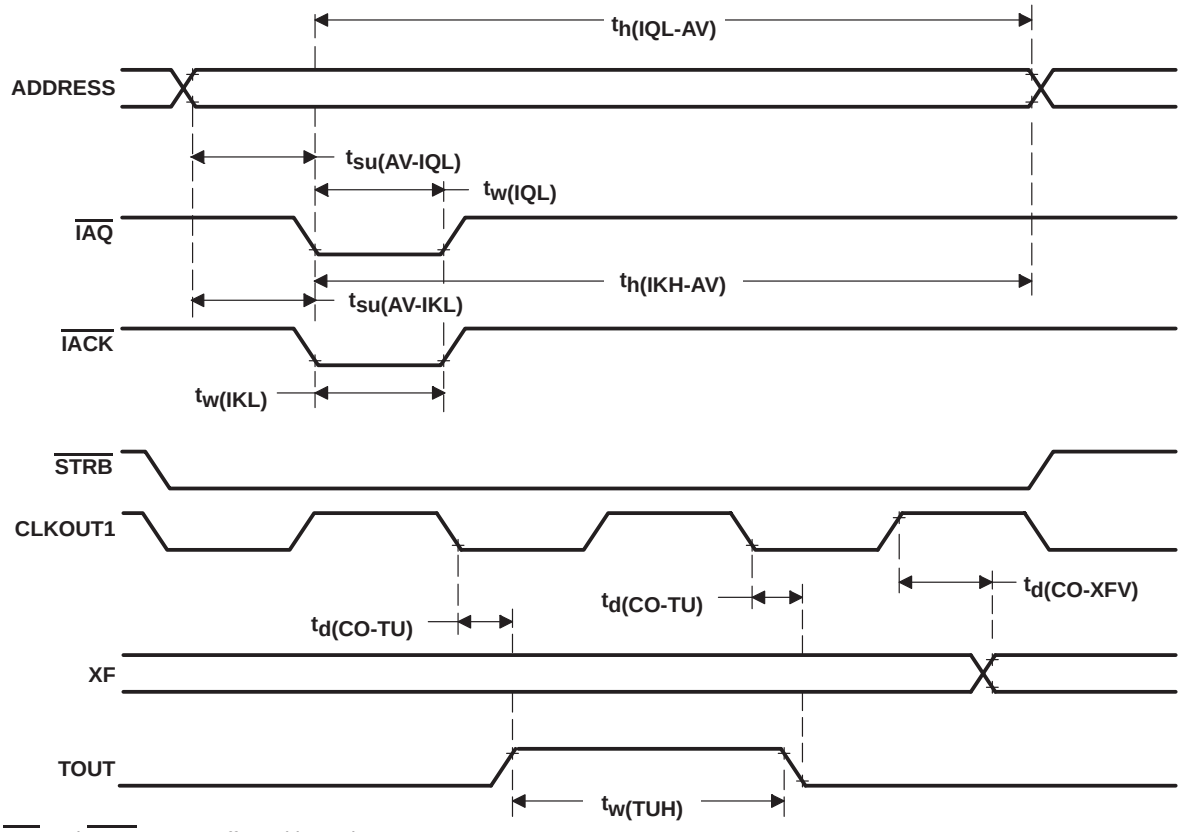
switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 12)

PARAMETER		MIN	MAX	UNIT
$t_{su(AV-IQL)}$	Setup time, address valid before $\overline{IAQ}$ low†	H−12‡		ns
$t_{h(IQL-AV)}$	Hold time, address valid after $\overline{IAQ}$ low	H−10‡		ns
$t_{w(IQL)}$	Pulse duration, $\overline{IAQ}$ low	H−10‡		ns
$t_{d(CO-TU)}$	Delay time, CLKOUT1 falling to TOUT	−6	6	ns
$t_{su(AV-IKL)}$	Setup time, address valid before $\overline{IACK}$ low§	H−12‡		ns
$t_{h(IKH-AV)}$	Hold time, address valid after $\overline{IACK}$ high §	H−10‡		ns
$t_{w(IKL)}$	Pulse duration, $\overline{IACK}$ low	H−10‡		ns
$t_{w(TUH)}$	Pulse duration, TOUT high	2H−12		ns
$t_{d(CO-XFV)}$	Delay time, XF valid after CLKOUT1	0	12	ns

† $\overline{IAQ}$ goes low during an instruction acquisition. It goes low only on the first cycle of the read when wait states are used. The falling edge should be used to latch the valid address. The AVIS bit in the PMST register must be set to zero for the address to be valid when the instruction being addressed resides in on-chip memory.

‡ Valid only if the external address reflects the current instruction activity (that is, code is executing on chip with no external bus cycles and AVIS is on, or code is executing off-chip)

§ $\overline{IACK}$ goes low during the fetch of the first word of the interrupt vector. It goes low only on the first cycle of the read when wait states are used. Address pins A1 − A4 can be decoded at the falling edge to identify the interrupt being acknowledged. The AVIS bit in the PMST register must be set to zero for the address to be valid when the vectors reside in on-chip memory.



NOTE: $\overline{IAQ}$ and $\overline{IACK}$ are not affected by wait states.

Figure 12. $\overline{IAQ}$, $\overline{IACK}$, and XF Timings Example With Two External Wait States

EXTERNAL DMA TIMING

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Note 3 and Figure 13)

PARAMETER		MIN	MAX	UNIT
$t_{d(HOL-HAL)}$	Delay time, $\overline{HOLD}$ low to $\overline{HOLDA}$ low	4H	†	ns
$t_{d(HOH-HAH)}$	Delay time, $\overline{HOLD}$ high before $\overline{HOLDA}$ high	2H		ns
$t_{dis(AZ-HAL)}$	Disable time, address in the high-impedance state before $\overline{HOLDA}$ low	H−15‡*		ns
$t_{en(HAH-Ad)}$	Enable time, $\overline{HOLDA}$ high to address driven	H−5*		ns
$t_{d(XBL-IQL)}$	Delay time, $\overline{XBR}$ low to $\overline{IAQ}$ low	4H*	6H*	ns
$t_{d(XBH-IQH)}$	Delay time, $\overline{XBR}$ high to $\overline{IAQ}$ high	2H*	4H*	ns
$t_{d(XSL-RDV)}$	Delay time, read data valid after $\overline{XSTRB}$ low		40	ns
$t_{h(XSH-RD)}$	Hold time, read data after $\overline{XSTRB}$ high	0		ns
$t_{en(IQL-RDd)}$	Enable time, $\overline{IAQ}$ low to read data driven	0*§	2H*	ns
$t_{dis(W)}$	Disable time, XR/$\overline{W}$ low to data in the high-impedance state	0*	15*	ns
$t_{dis(I-D)}$	Disable time, $\overline{IAQ}$ high to data in the high-impedance state		H*	ns
$t_{en(D-XRH)}$	Enable time, data from XR/$\overline{W}$ going high		4*	ns

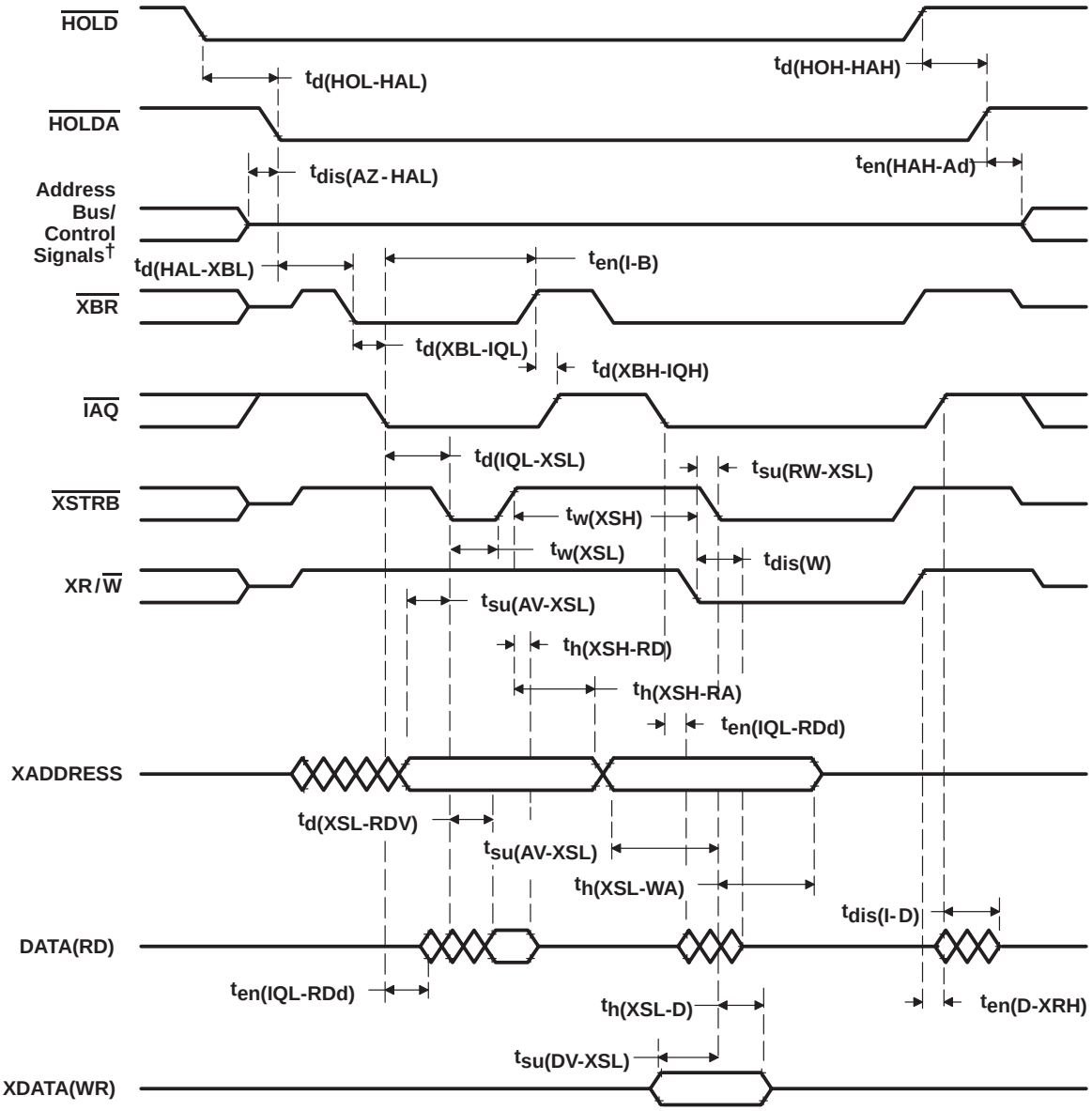
† $\overline{HOLD}$ is not acknowledged until current external access request is complete.
‡ This parameter includes all memory control lines.
§ This parameter refers to the delay between the time the condition ($\overline{IAQ}$ = 0 and XR/$\overline{W}$ = 1) is satisfied and the time that the 320C50x data lines become valid.
* This parameter is not production tested.
NOTE 3: X preceding a name refers to the external drive of the signal.

timing requirements (see Note 3 and Figure 13)

		MIN	MAX	UNIT
$t_{d(HAL-XBL)}$	Delay time, $\overline{HOLDA}$ low to $\overline{XBR}$ low	0¶		ns
$t_{d(IQL-XSL)}$	Delay time, $\overline{IAQ}$ low to $\overline{XSTRB}$ low	0¶		ns
$t_{su(AV-XSL)}$	Setup time, Xaddress valid before $\overline{XSTRB}$ low	15		ns
$t_{su(DV-XSL)}$	Setup time, Xdata valid before $\overline{XSTRB}$ low	15		ns
$t_{h(XSL-D)}$	Hold time, Xdata hold after $\overline{XSTRB}$ low	15		ns
$t_{h(XSL-WA)}$	Hold time, write Xaddress hold after $\overline{XSTRB}$ low	15		ns
$t_{w(XSL)}$	Pulse duration, $\overline{XSTRB}$ low	45		ns
$t_{w(XSH)}$	Pulse duration, $\overline{XSTRB}$ high	45		ns
$t_{su(RW-XSL)}$	Setup time, R/$\overline{W}$ valid before $\overline{XSTRB}$ low	20		ns
$t_{h(XSH-RA)}$	Hold time, read Xaddress after $\overline{XSTRB}$ high	0		ns

¶ $\overline{XBR}$, XR/$\overline{W}$, and $\overline{XSTRB}$ lines should be pulled up with a 10-kΩ resistor to assure that they are in an inactive (high) state during the transition period between the 320C50x driving them and the external circuit driving them.
NOTE 3: X preceding a name refers to the external drive of the signal.

EXTERNAL DMA TIMING



† A15−A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in timings referenced as address bus/control signals.

Figure 13. External DMA Timing

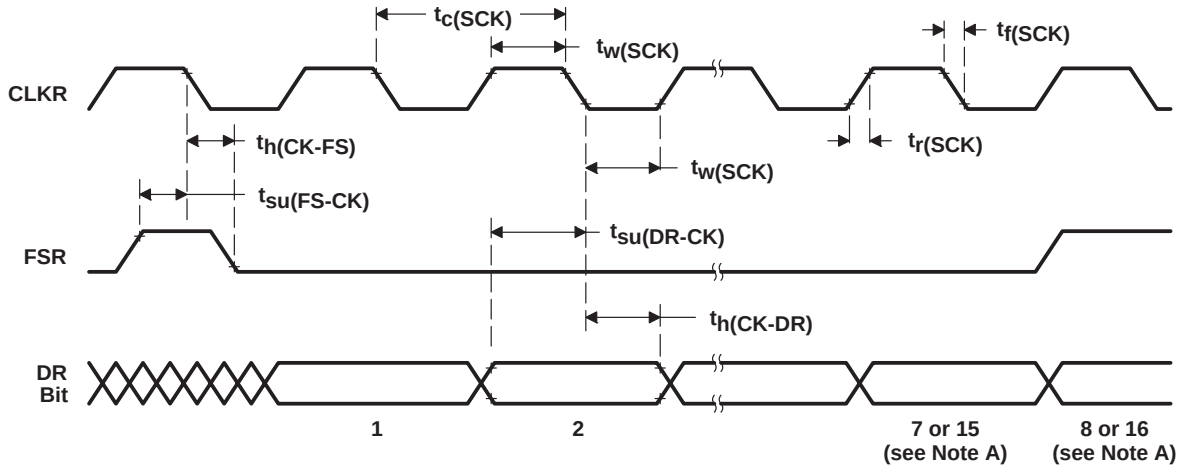
SERIAL-PORT RECEIVE

timing requirements [H = 0.5$t_{c(CO)}$] (see Figure 14)

		MIN	MAX	UNIT
$t_{c(SCK)}$	Cycle time, serial-port clock	5.2H	†	ns
$t_{f(SCK)}$	Fall time, serial-port clock		8*	ns
$t_{r(SCK)}$	Rise time, serial-port clock		8*	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	2.1H		ns
$t_{su(FS-CK)}$	Setup time, FSR before CLKR falling edge	10		ns
$t_{h(CK-FS)}$	Hold time, FSR after CLKR falling edge	10		ns
$t_{su(DR-CK)}$	Setup time, DR before CLKR falling edge	10		ns
$t_{h(CK-DR)}$	Hold time, DR after CLKR falling edge	10		ns

† The serial-port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

* This parameter is not production tested.



NOTE A: Depending on whether information is sent in an 8-bit or 16-bit packet.

Figure 14. Serial-Port Receive Timing

SERIAL-PORT TRANSMIT, EXTERNAL CLOCKS AND EXTERNAL FRAMES

switching characteristics over recommended operating conditions (see Note 4 and Figure 15)

PARAMETER		MIN	MAX	UNIT
$t_{d(CXH-DXV)}$	Delay time, DX valid after CLKX high		25	ns
$t_{dis(CXH-DX)}$	Disable time, DX valid after CLKX high		40*	ns
$t_{h(CXH-DXV)}$	Hold time, DX valid after CLKX high	−5		ns

* This parameter is not production tested.

NOTE 4: Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX are always defined depending on the source of FSX, and CLKX timings are always dependent upon the source of CLKX. Specifically, the relationship of FSX to CLKX is independent of the source of CLKX.

timing requirements [H = 0.5$t_{c(CO)}$] (see Note 4 and Figure 15)

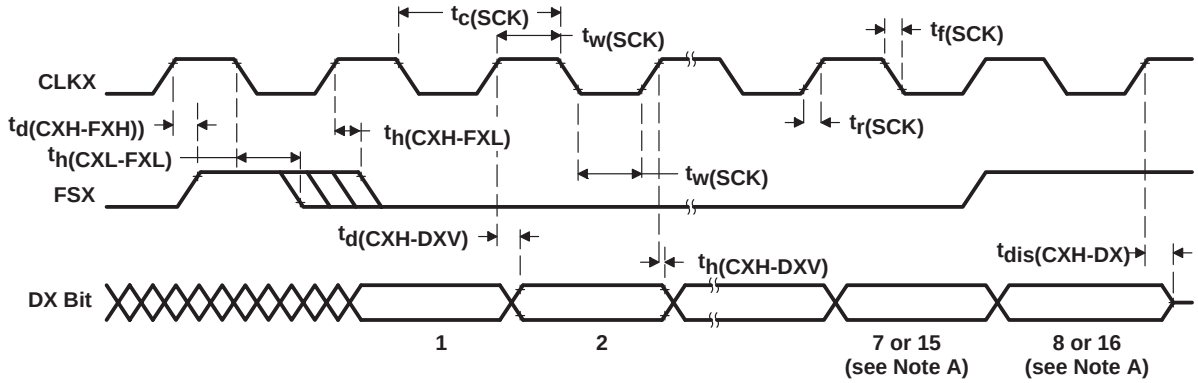
		MIN	MAX	UNIT
$t_{c(SCK)}$	Cycle time, serial-port clock	5.2H	†	ns
$t_{f(SCK)}$	Fall time, serial-port clock		8*	ns
$t_{r(SCK)}$	Rise time, serial-port clock		8*	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	2.1H		ns
$t_{d(CXH-FXH)}$	Delay time, FSX after CLKX high edge		2H−8	ns
$t_{h(CXL-FXL)}$	Hold time, FSX after CLKX falling edge	10		ns
$t_{h(CXH-FXL)}$	Hold time, FSX after CLKX high edge		2H−8‡*	ns

† The serial-port design is fully static and therefore can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

‡ If the FSX pulse does not meet this specification, the first bit of serial data is driven on the DX pin until the falling edge of FSX. After the falling edge of FSX, data is shifted out on the DX pin. The transmit-buffer-empty interrupt is generated when the $t_{h(FS)}$ and $t_{h(FS)H}$ specification is met.

NOTE 4: Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX are always defined depending on the source of FSX, and CLKX timings are always dependent upon the source of CLKX. Specifically, the relationship of FSX to CLKX is independent of the source of CLKX.

* This parameter is not production tested.



NOTE A: Depending on whether information is sent in an 8-bit or 16-bit packet

Figure 15. Serial-Port Transmit Timing of External Clocks and External Frames

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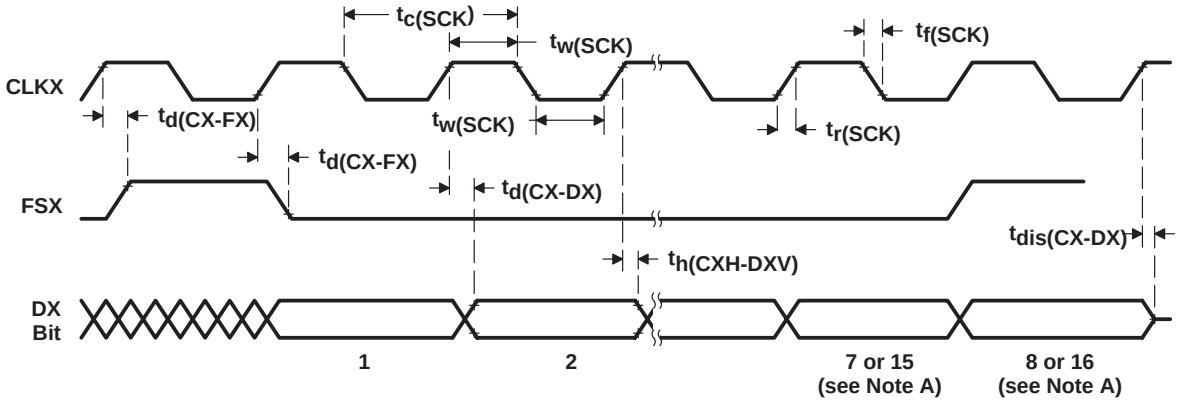
SERIAL-PORT TRANSMIT, INTERNAL CLOCKS AND INTERNAL FRAMES

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Note 4 and Figure 16)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(CX-FX)}$	Delay time, CLKX rising to FSX			25	ns
$t_{d(CX-DX)}$	Delay time, CLKX rising to DX			25	ns
$t_{dis(CX-DX)}$	Disable time, CLKX rising to DX			40*	ns
$t_{c(SCK)}$	Cycle time, serial-port clock		8H		ns
$t_{f(SCK)}$	Fall time, serial-port clock		5		ns
$t_{r(SCK)}$	Rise time, serial-port clock		5		ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	4H − 20			ns
$t_{h(CXH-DXV)}$	Hold time, DX valid after CLKX high	− 6			ns

* This parameter is not production tested.

NOTE 4: Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX are always defined depending on the source of FSX, and CLKX timings are always dependent upon the source of CLKX. Specifically, the relationship of FSX to CLKX is independent of the source of CLKX.



NOTE A: Depending on whether information is sent in an 8-bit or 16-bit packet

Figure 16. Serial-Port Transmit Timing of Internal Clocks and Internal Frames

SERIAL-PORT RECEIVE TIMING IN TDM MODE

timing requirements [H = 0.5$t_{c(CO)}$] (see Figure 17)

		MIN	MAX	UNIT
$t_{c(SCK)}$	Cycle time, serial-port clock	5.2H	†	ns
$t_{f(SCK)}$	Fall time, serial-port clock		8*	ns
$t_{r(SCK)}$	Rise time, serial-port clock		8*	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	2.1H		ns
$t_{su(TD-TCH)}$	Setup time, TDAT/TADD before TCLK rising	30		ns
$t_{h(TCH-TD)}$	Hold time, TDAT/TADD after TCLK rising	−3		ns
$t_{su(TA-TCH)}$	Setup time, TDAT/TADD before TCLK rising‡	20		ns
$t_{h(TCH-TA)}$	Hold time, TDAT/TADD after TCLK rising‡	− 3		ns
$t_{su(TF-TCH)}$	Setup time, TRFM before TCLK rising edge§	10		ns
$t_{h(TCH-TF)}$	Hold time, TRFM after TCLK rising edge§	10		ns

† The serial-port design is fully static and therefore can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.
‡ These parameters apply only to the first bits in the serial bit string.
§ TFRM timing and waveforms shown in Figure 17 are for external TFRM. TFRM also can be configured as internal. The TFRM internal case is illustrated in the transmit timing diagram in Figure 18.
* This parameter is not production tested.

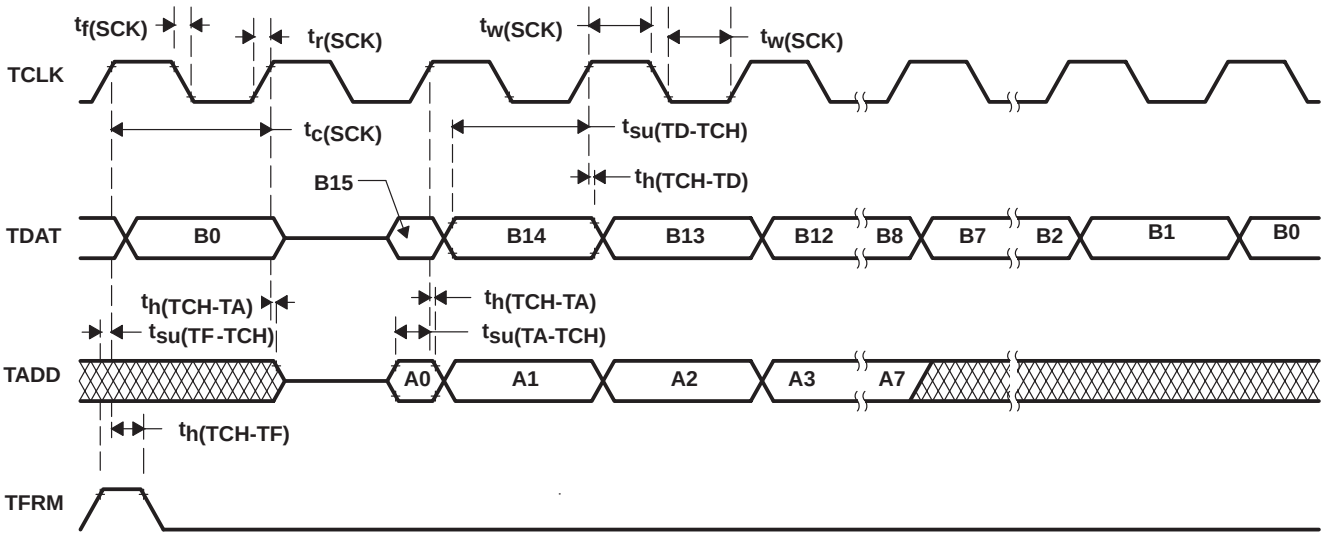


Figure 17. Serial-Port Receive Timing in TDM Mode

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SERIAL-PORT TRANSMIT TIMING IN TDM MODE

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 18)

PARAMETER		MIN	MAX	UNIT
$t_{h(TCH-TDV)}$	Hold time, TDAT/TADD valid after TCLK rising	0		ns
$t_{d(TCH-TFV)}$	Delay time, TFRM valid after TCLK rising†	H	3H+10	ns
$t_{d(TC-TDV)}$	Delay time, TCLK to valid TDAT/TADD		20	ns

† TFRM timing and waveforms shown in Figure 18 are for internal TFRM. TFRM can also be configured as external, and the TFRM external case is illustrated in the receive timing diagram in Figure 17.

timing requirements [H = 0.5$t_{c(CO)}$] (see Figure 18)

		MIN	TYP	MAX	UNIT
$t_{c(SCK)}$	Cycle time, serial-port clock	5.2H	8H‡	§	ns
$t_{f(SCK)}$	Fall time, serial-port clock			8*	ns
$t_{r(SCK)}$	Rise time, serial-port clock			8*	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	2.1H			ns

‡ When SCK is generated internally.
§ The serial-port design is fully static and therefore can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.
* This parameter is not production tested.

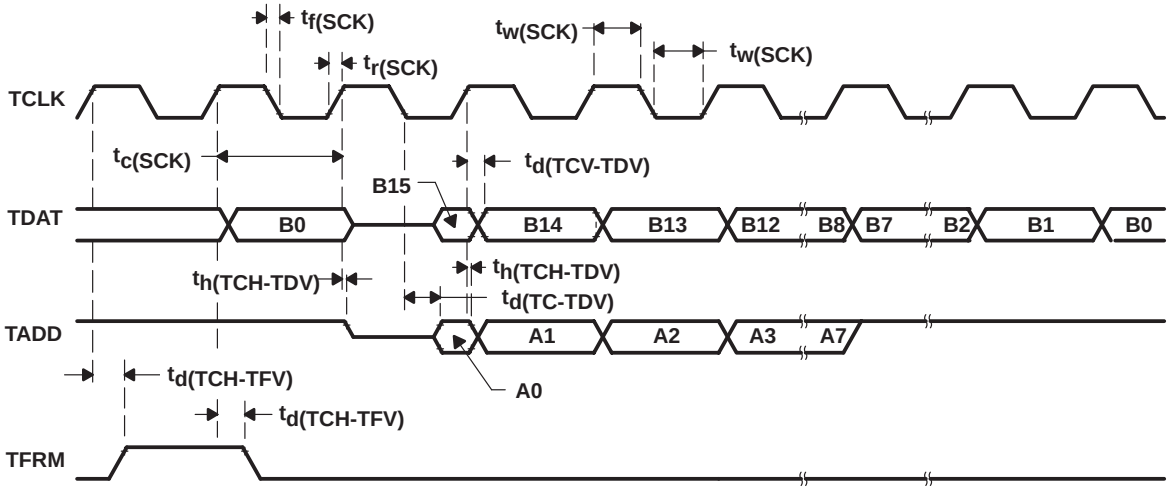


Figure 18. Serial-Port Transmit Timing in TDM Mode

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SM320C50PQI80EP	NRND	BQFP	PQ	132	36	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	
SM320C50PQM66EP	NRND	BQFP	PQ	132	36	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	
V62/03613-01XE	NRND	BQFP	PQ	132	36	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	
V62/03613-02XE	NRND	BQFP	PQ	132	36	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SM320C50-EP :

- Catalog: SM320C50

NOTE: Qualified Version Definitions:

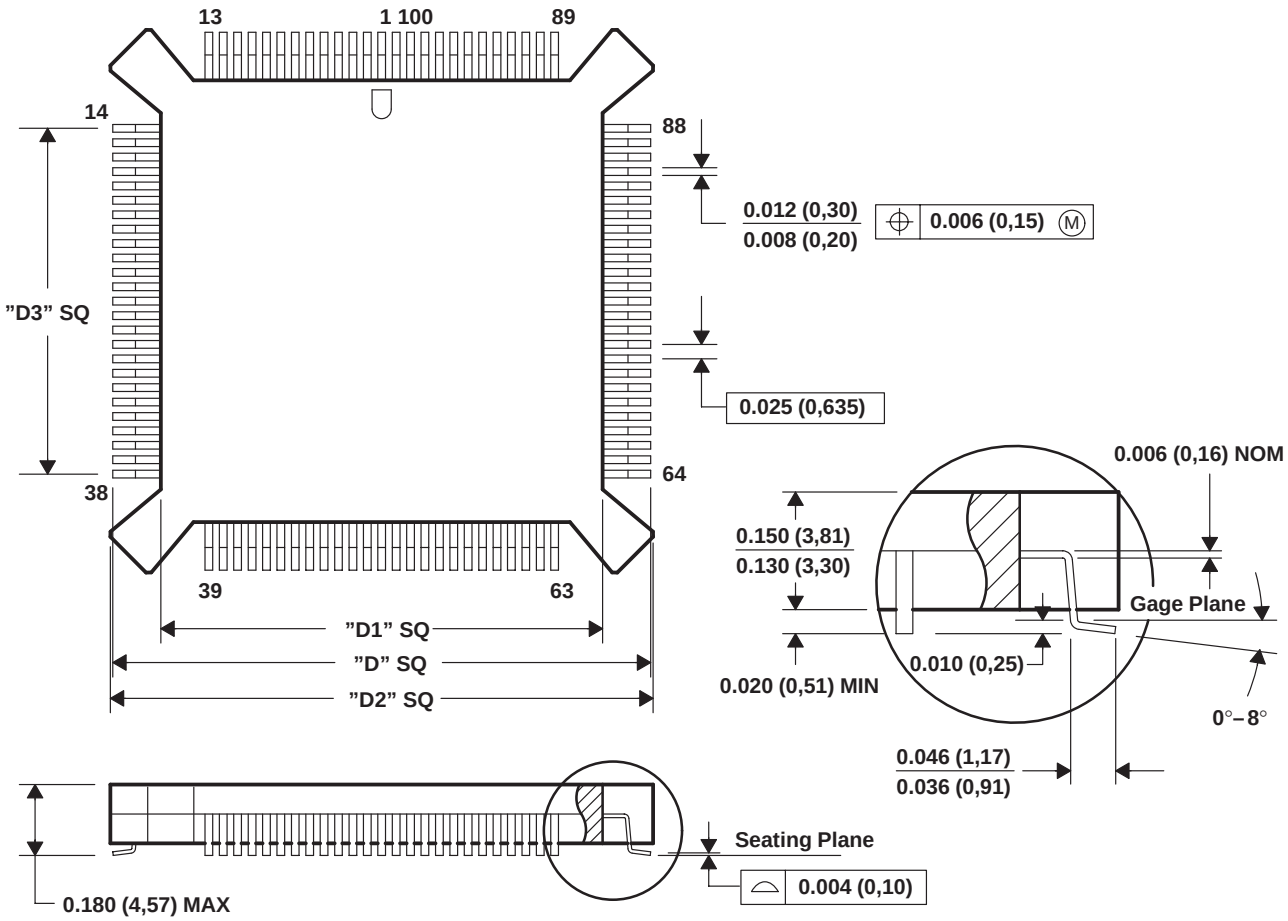
- Catalog - TI's standard catalog product

MBQF001A – NOVEMBER 1995

PQ (S-PQFP-G***)

PLASTIC QUAD FLATPACK

100 LEAD SHOWN



DIM \ LEADS ***		100	132
"D"	MAX	0.890 (22,61)	1.090 (27,69)
	MIN	0.870 (22,10)	1.070 (27,18)
"D1"	MAX	0.766 (19,46)	0.966 (24,54)
	MIN	0.734 (18,64)	0.934 (23,72)
"D2"	MAX	0.912 (23,16)	1.112 (28,25)
	MIN	0.888 (22,56)	1.088 (27,64)
"D3"	NOM	0.600 (15,24)	0.800 (20,32)

4040045/C 11/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-069

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